

Fig. 1

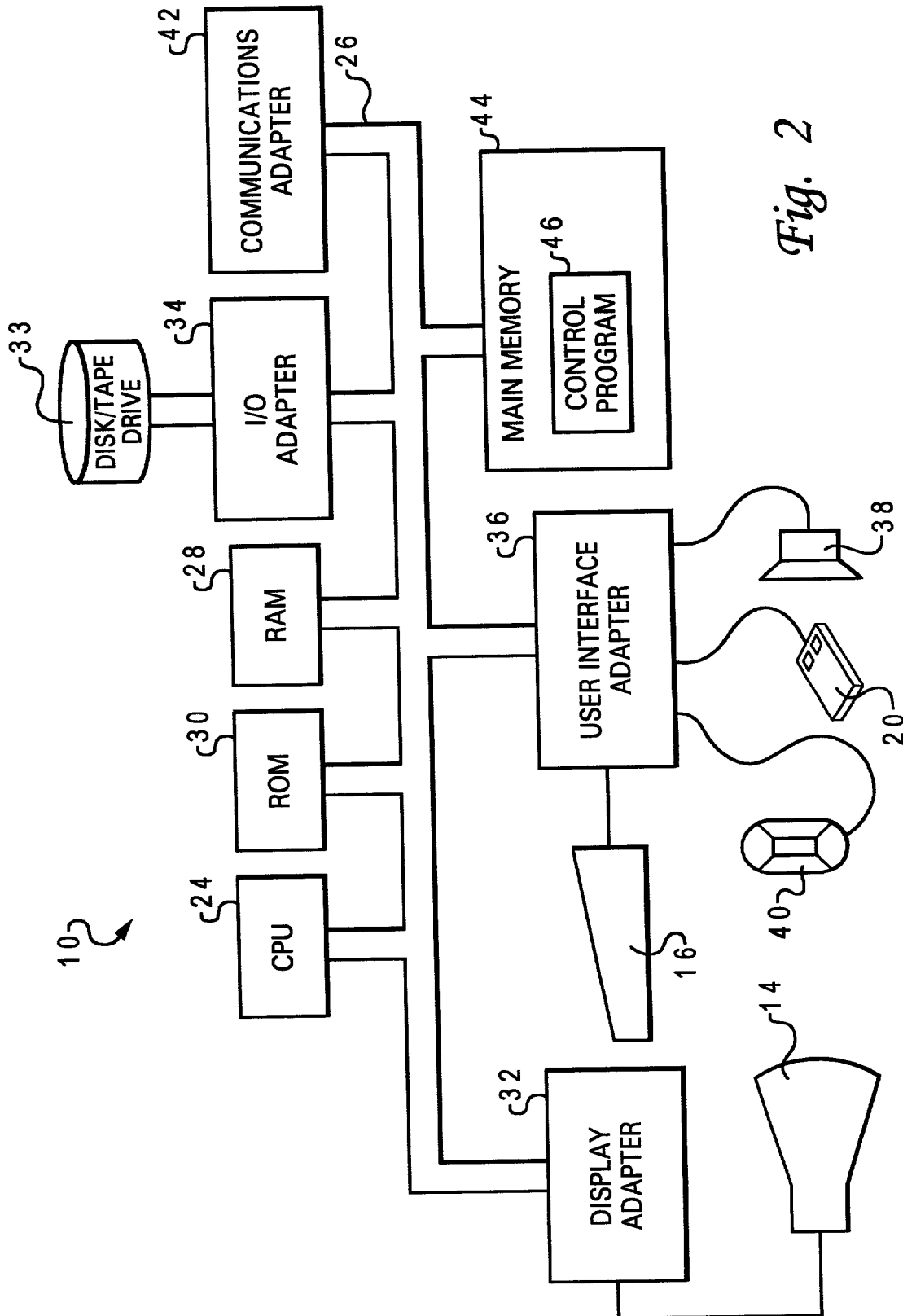


Fig. 2

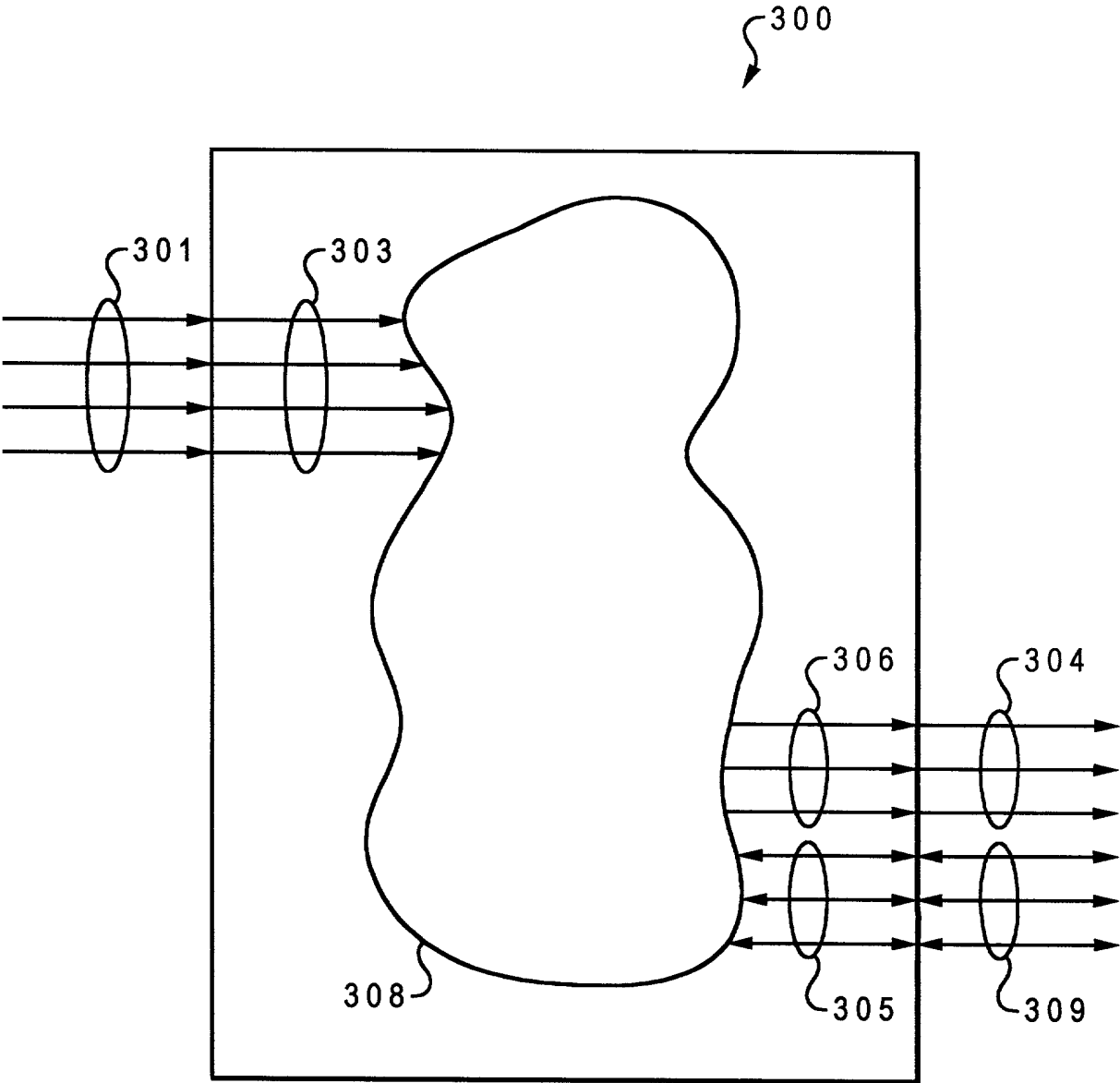


Fig. 3A

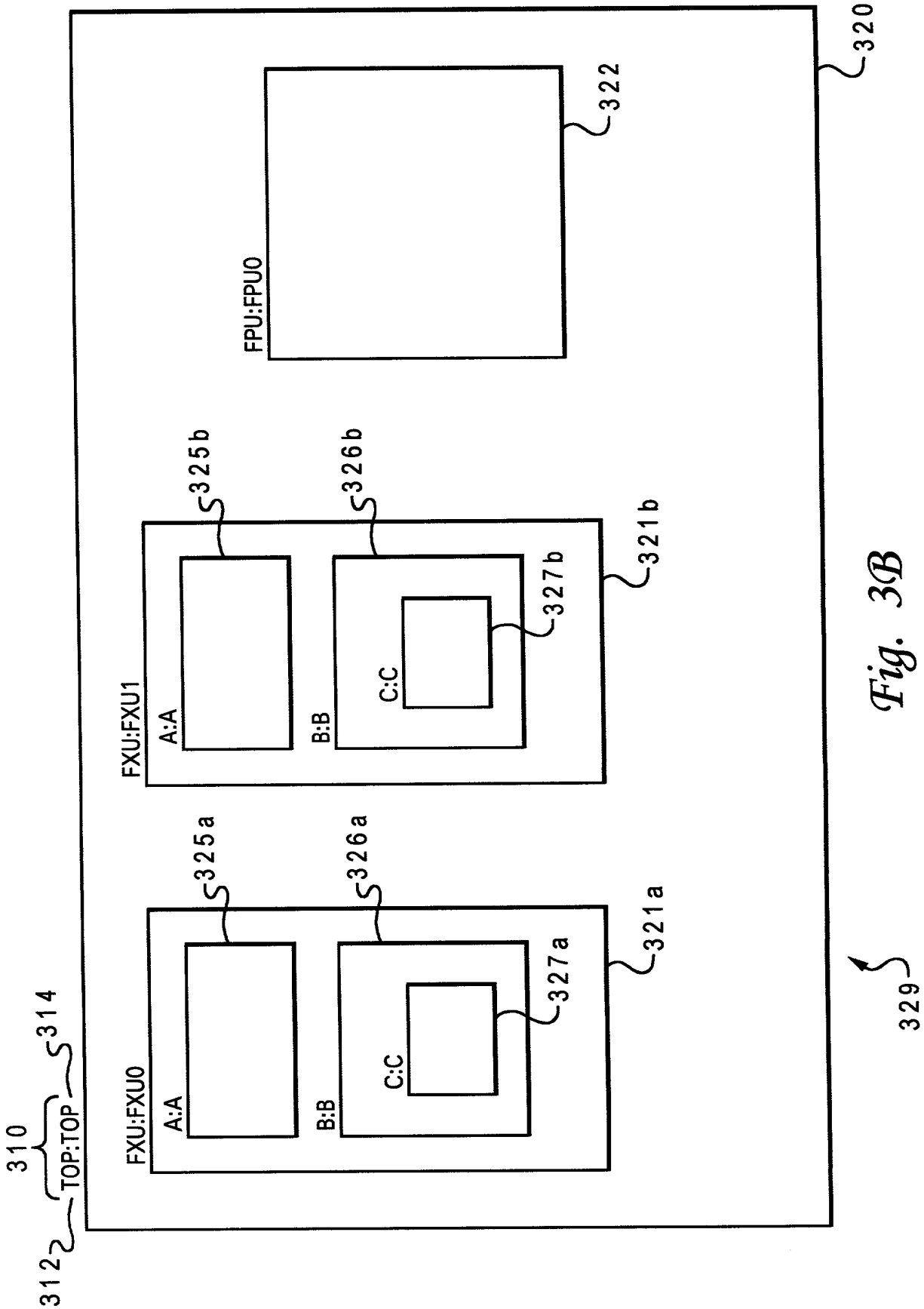
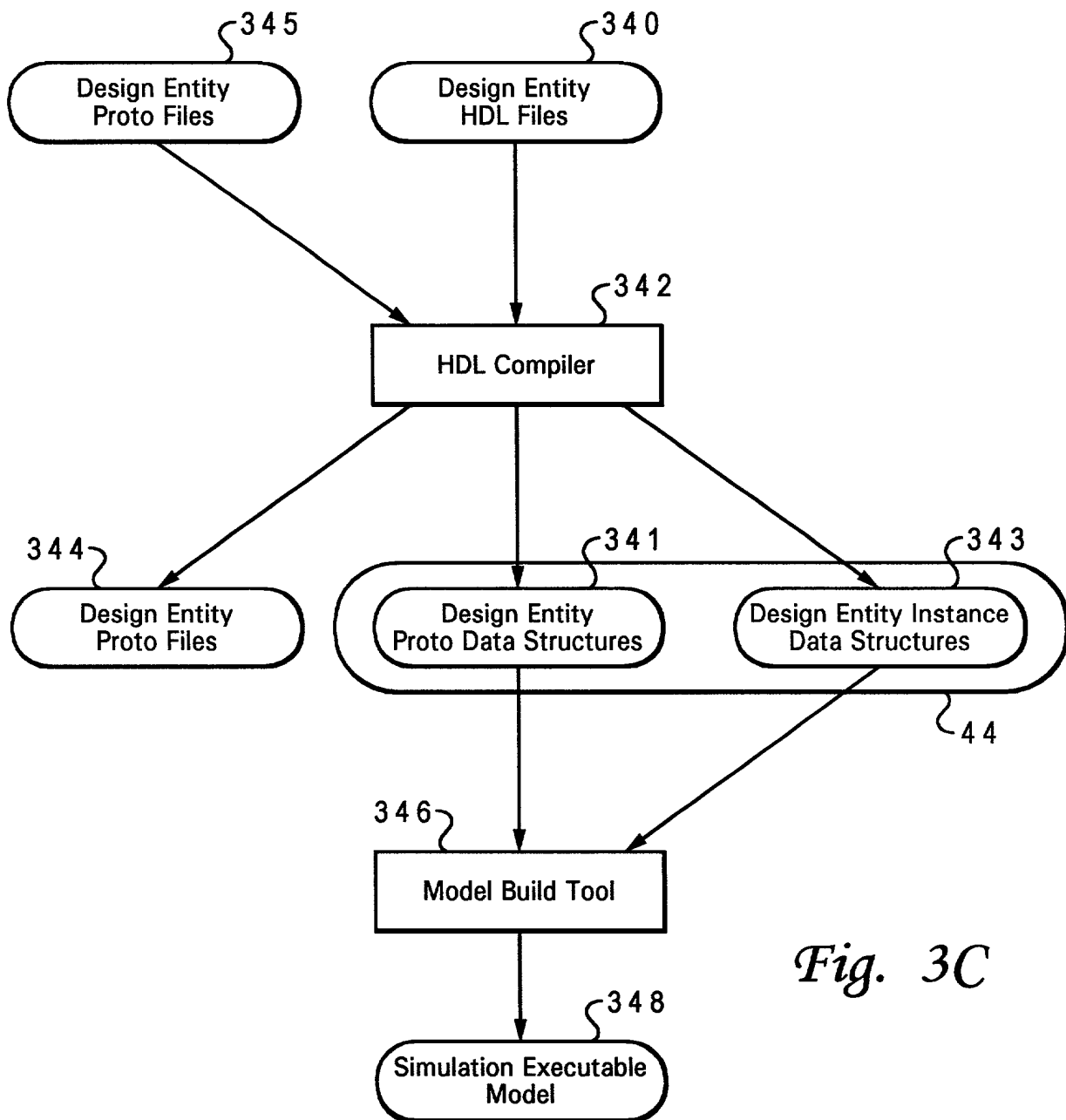


Fig. 3B

*Fig. 3C*

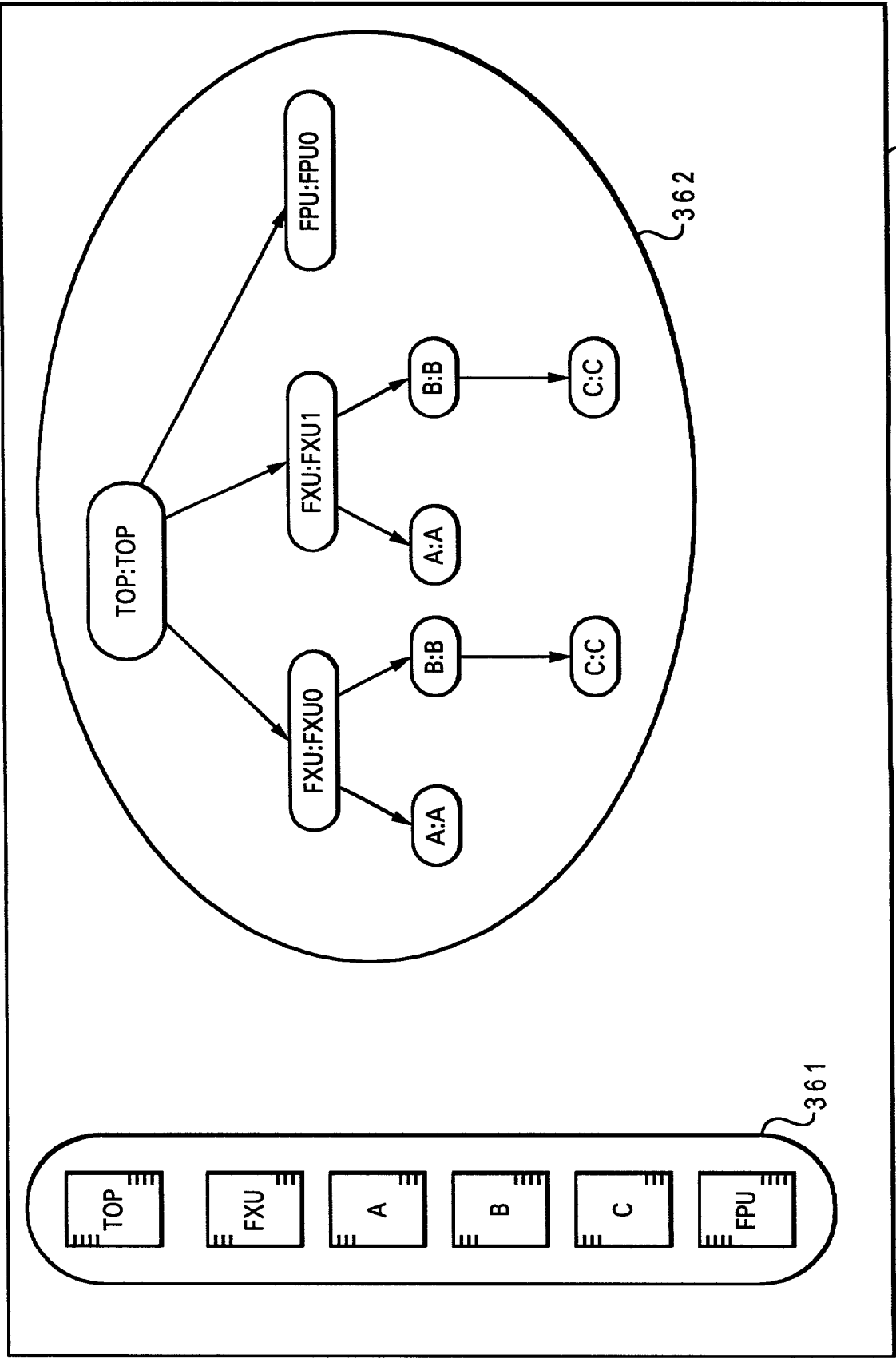
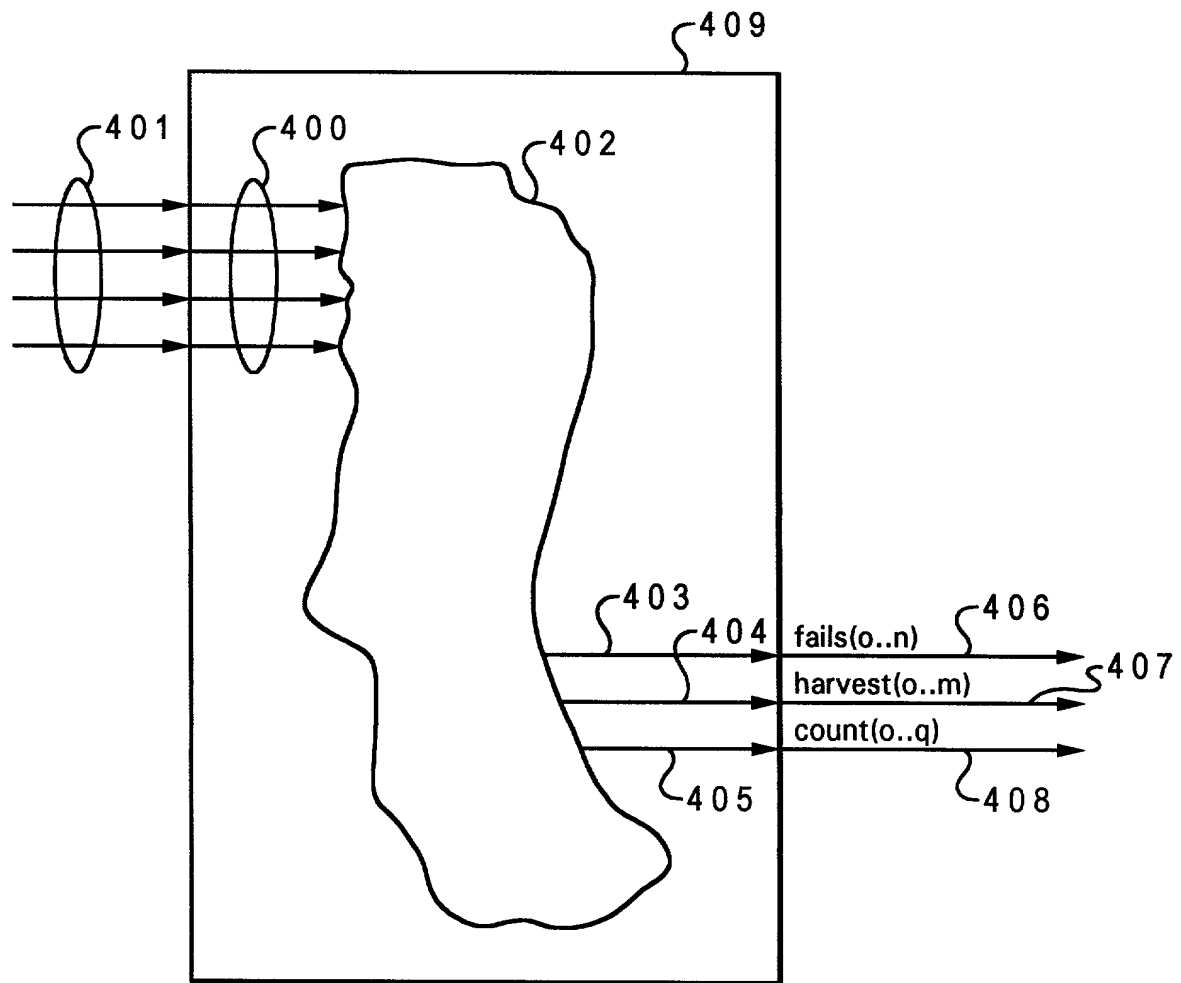


Fig. 3D

*Fig. 4A*

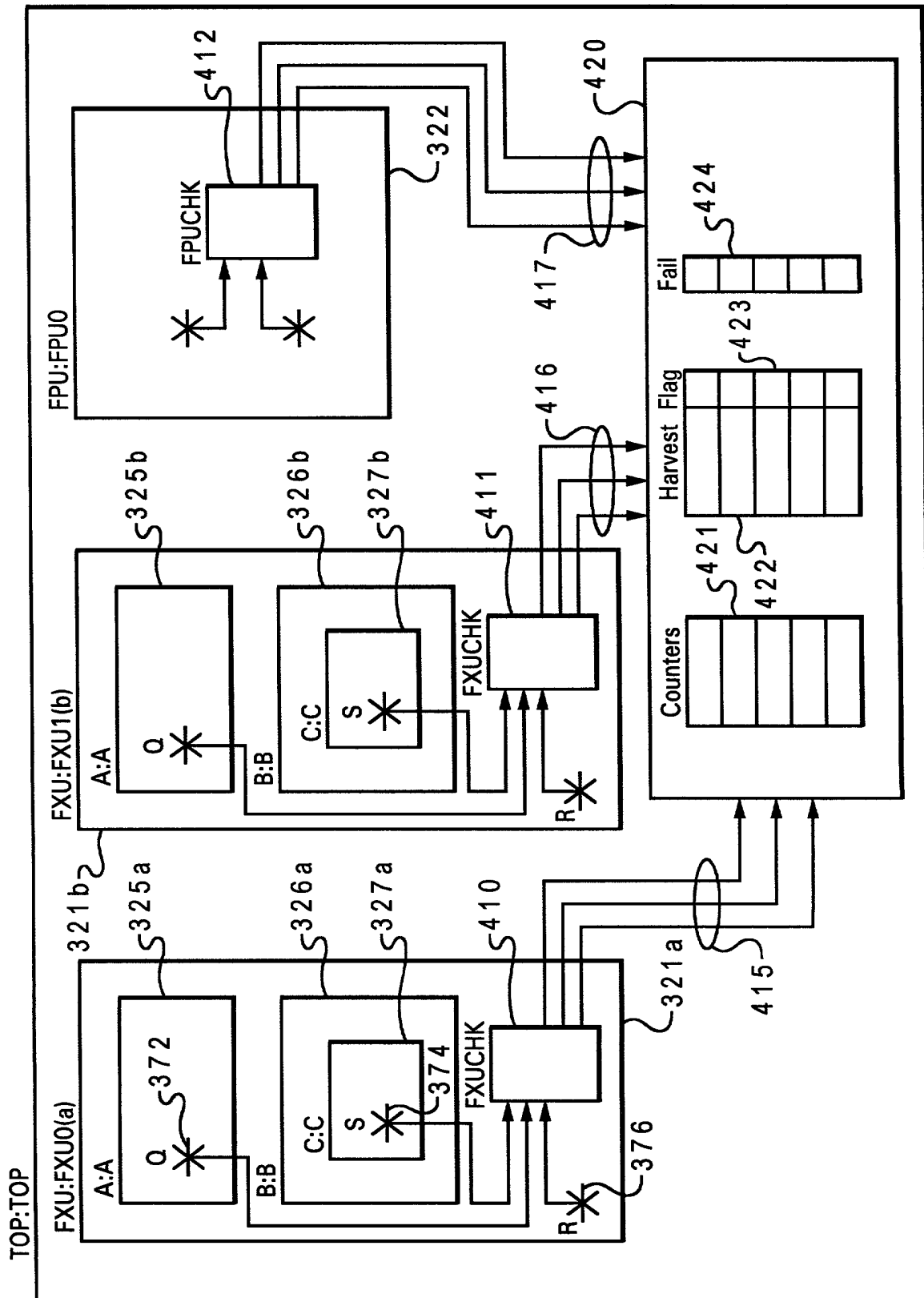


Fig. 4B

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```

ENTITY FXUCHK IS
    PORT(
        S_IN      : IN std_ulogic;
        Q_IN      : IN std_ulogic;
        R_IN      : IN std_ulogic;
        clock      : IN std_ulogic;
        fails      : OUT std_ulogic_vector(0 to 1);
        counts     : OUT std_ulogic_vector(0 to 2);
        harvests   : OUT std_ulogic_vector(0 to 1);
    );
4 5 2 { --!! BEGIN
      --!! Design Entity: FXU;

4 5 3 { --!! Inputs
      --!! S_IN      => B.C.S;
      --!! Q_IN      => A.Q;
      --!! R_IN      => R;
      --!! CLOCK     => clock;
      --!! End Inputs

4 5 4 { --!! Fail Outputs;
      --!! 0 : "Fail message for failure event 0";
      --!! 1 : "Fail message for failure event 1";
      --!! End Fail Outputs;

4 5 5 { --!! Count Outputs;
      --!! 0 : <event0> clock;
      --!! 1 : <event1> clock;
      --!! 2 : <event2> clock;
      --!! End Count Outputs;

4 5 6 { --!! Harvest Outputs;
      --!! 0 : "Message for harvest event 0";
      --!! 1 : "Message for harvest event 1";
      --!! End Harvest Outputs;

4 5 7 { --!! End;

    ARCHITECTURE example of FXUCHK IS
        BEGIN
            ... HDL code for entity body section ...
        END;

```

4 5 0

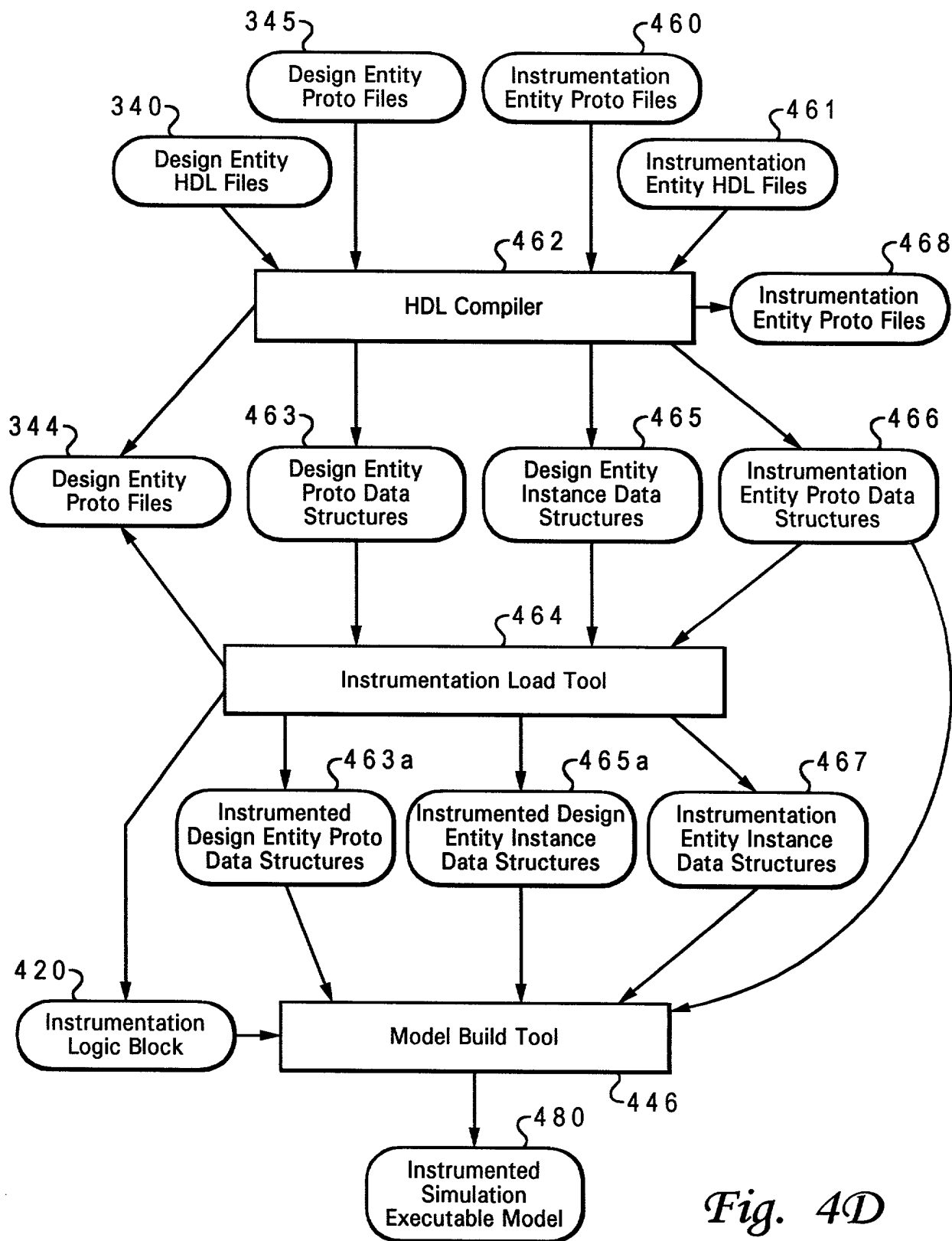
4 5 1

4 4 0

4 5 8

Fig. 4C

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*Fig. 4D*

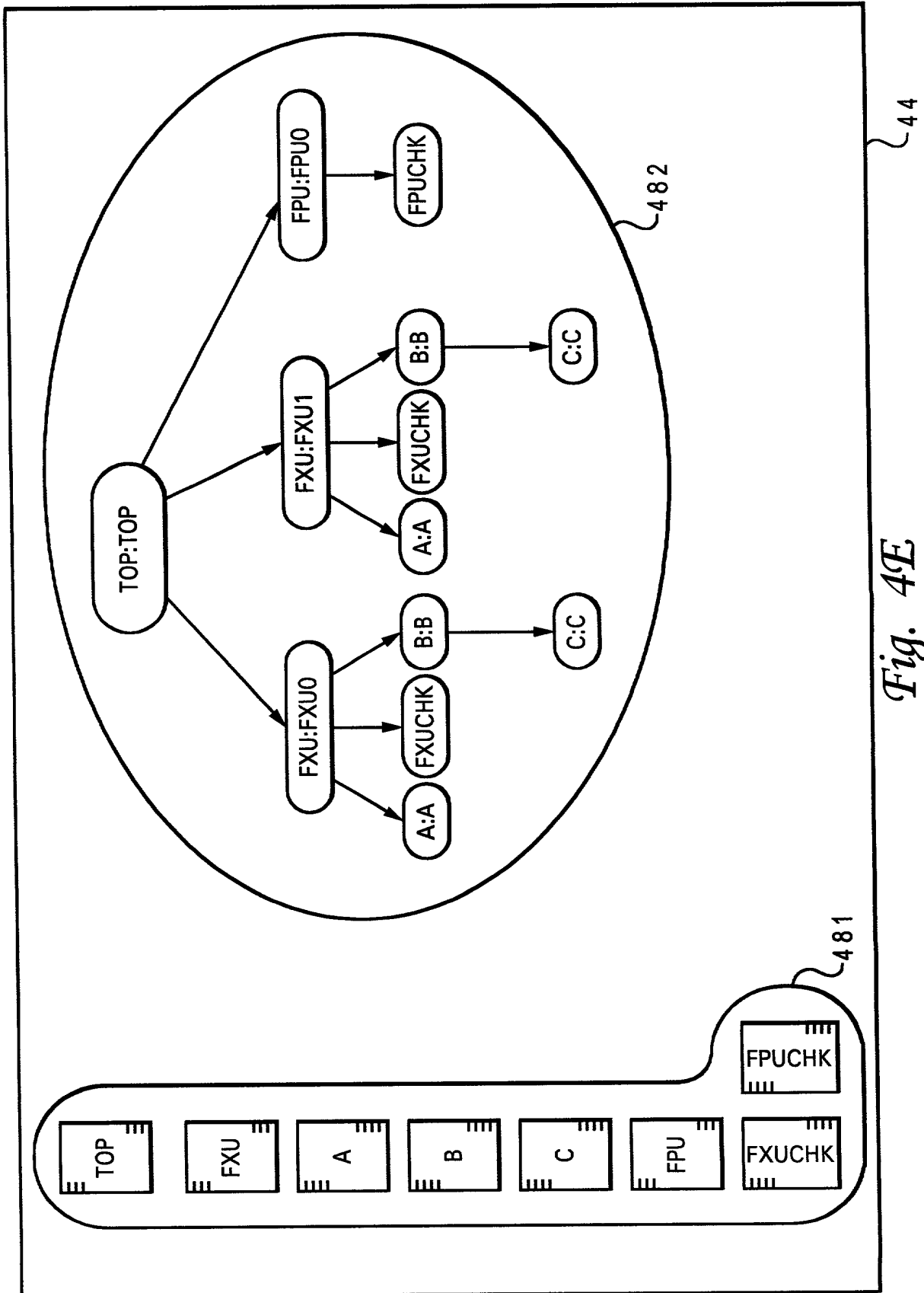


Fig. 4E

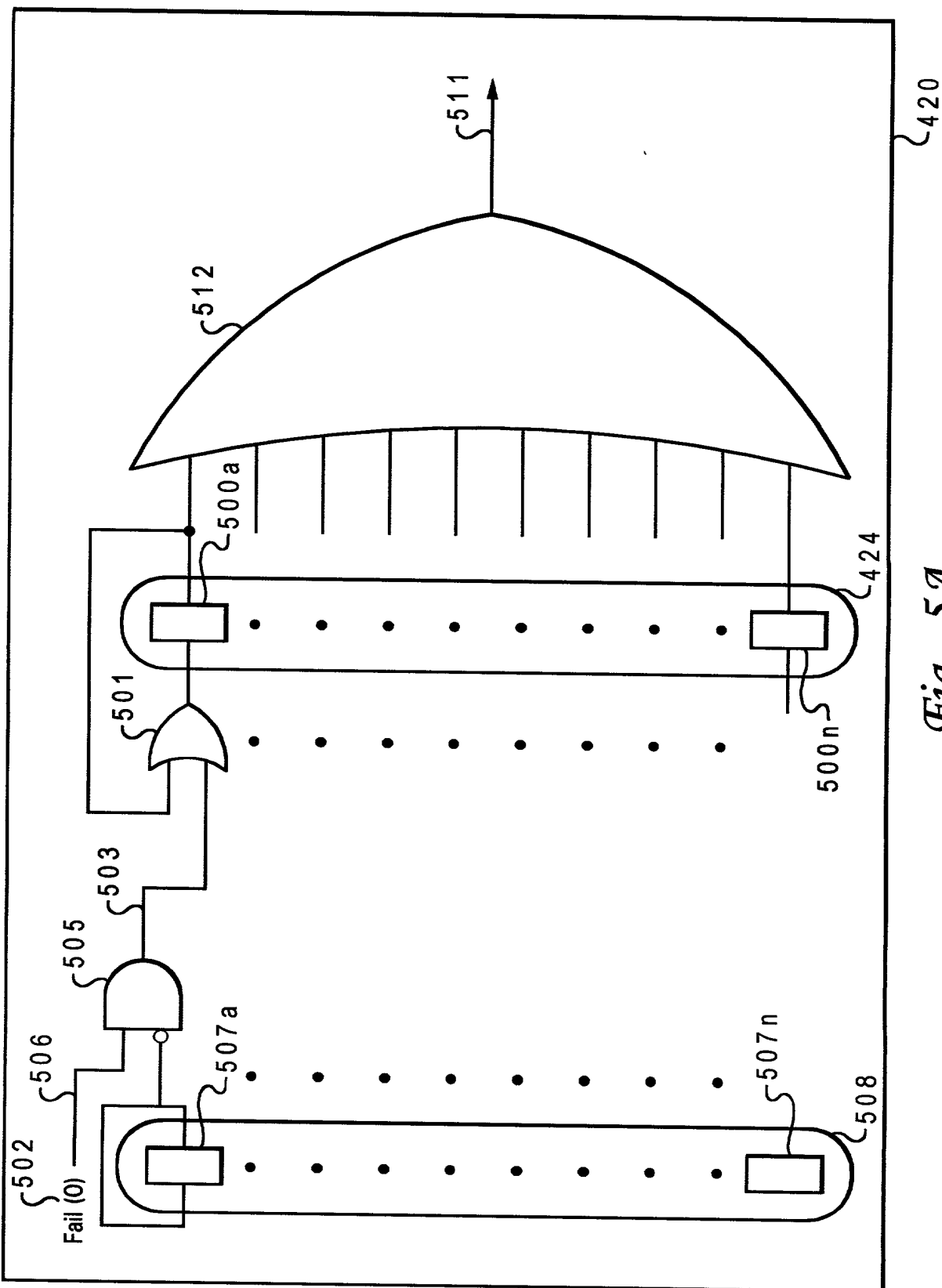


Fig. 5A

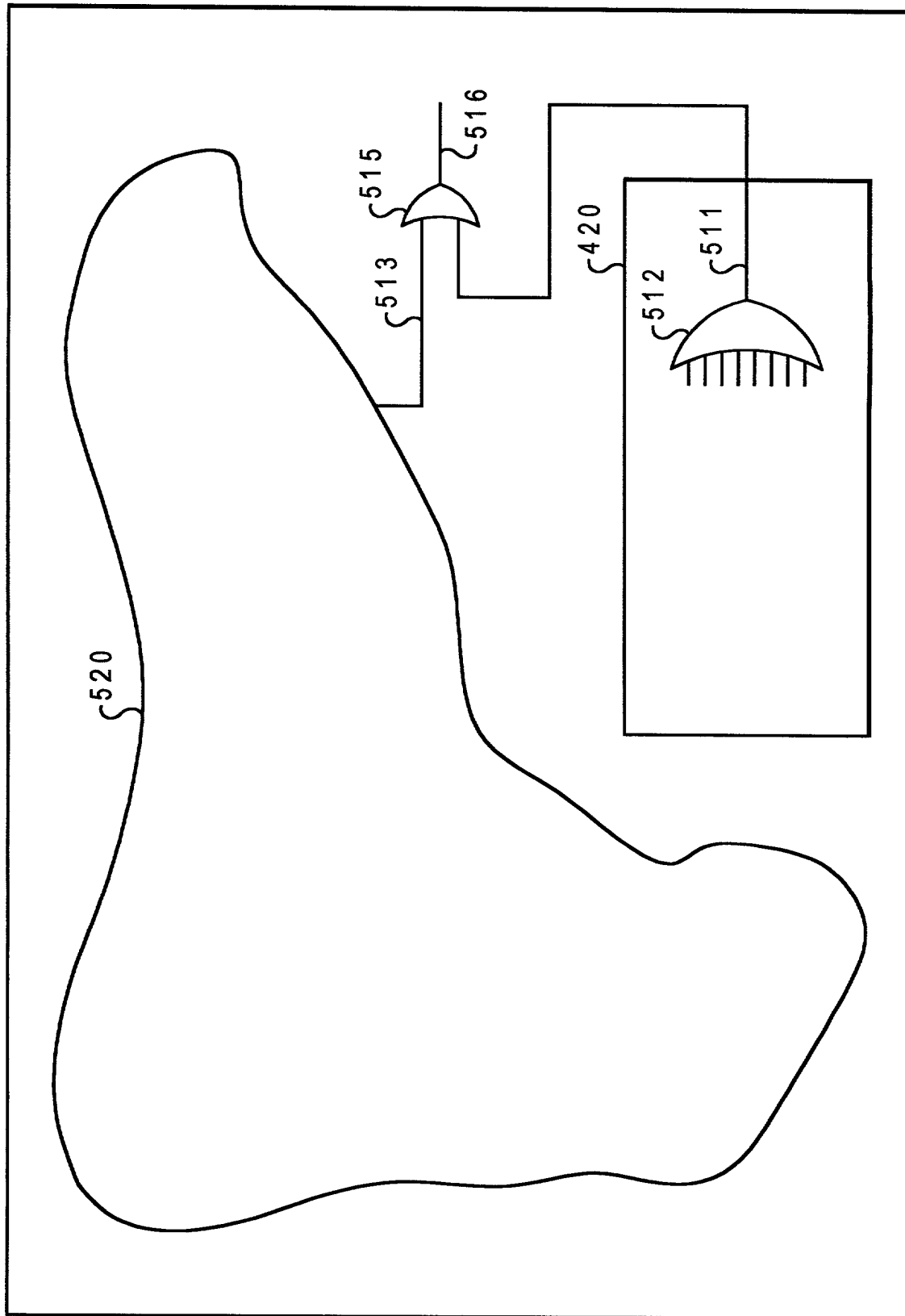


Fig. 5B

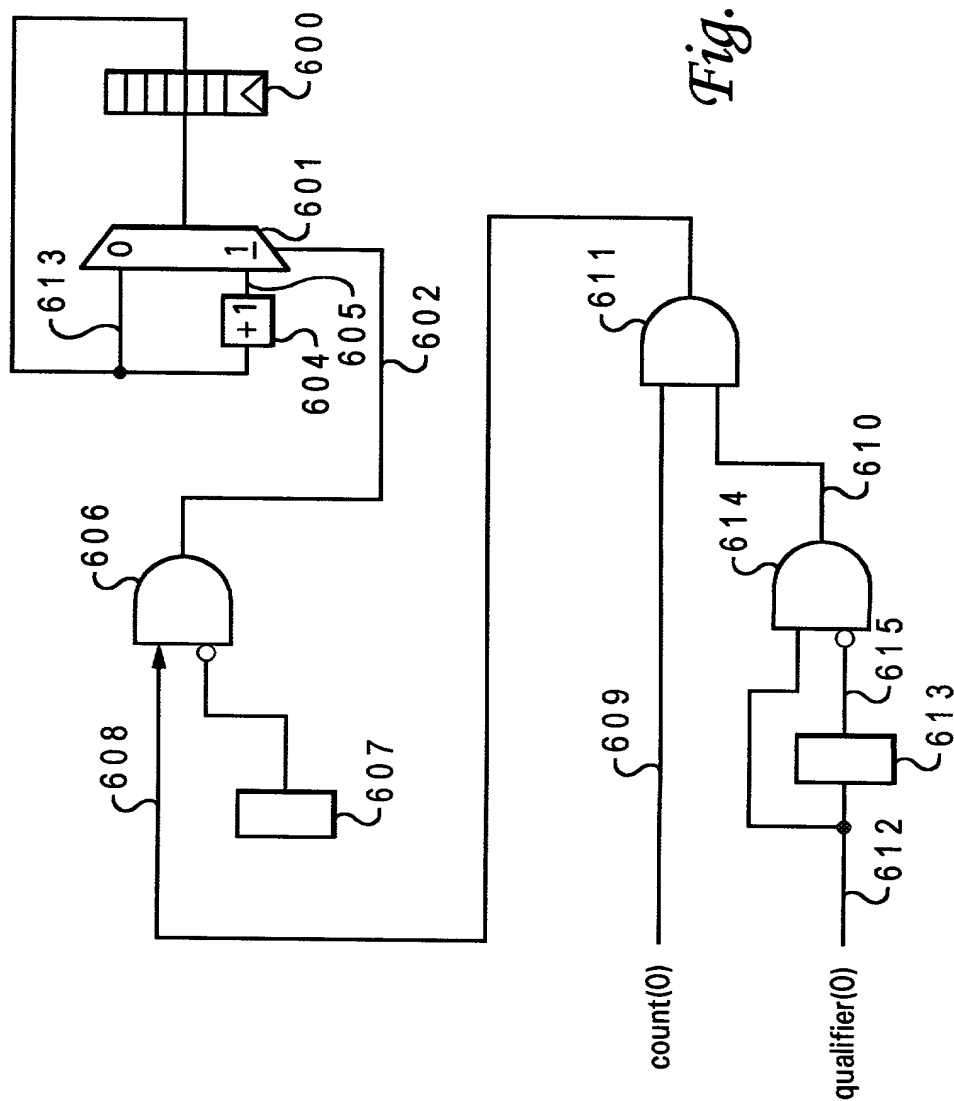


Fig. 6A

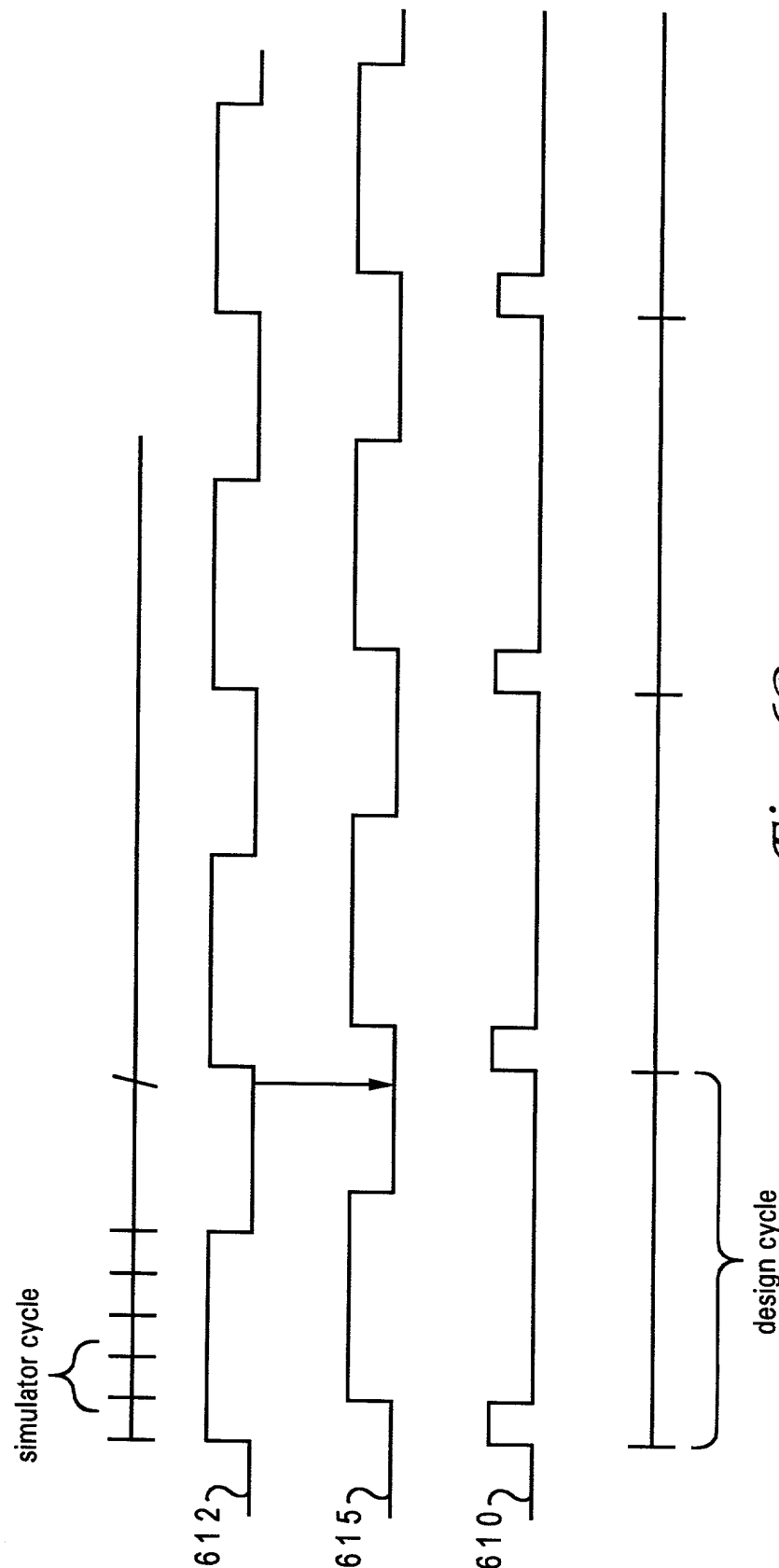


Fig. 6B

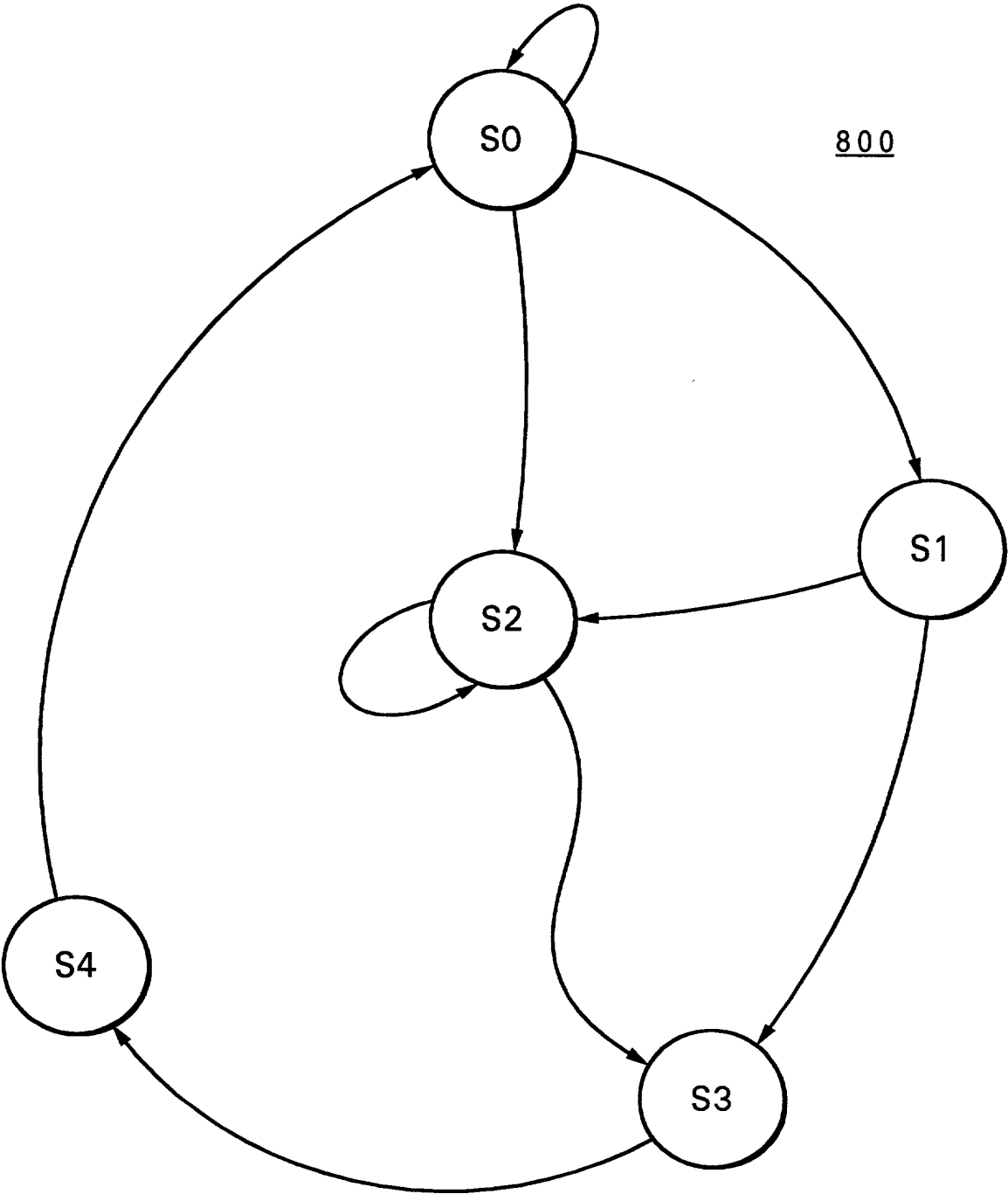


Fig. 8A
Prior Art

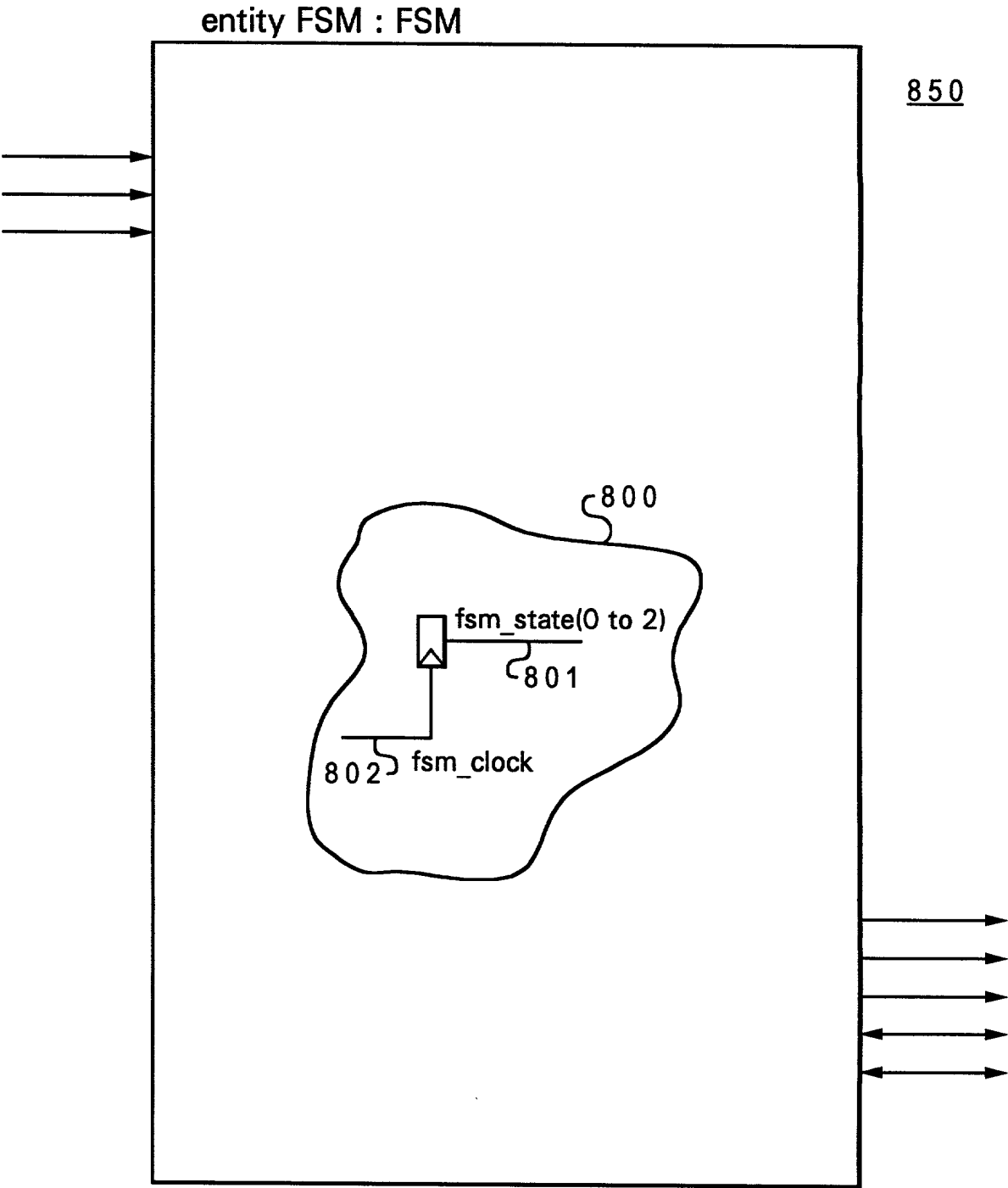


Fig. 8B
Prior Art

ENTITY FSM IS

```
PORT(
    ....ports for entity fsm....
);
```

ARCHITECTURE FSM OF FSM IS

BEGIN

... HDL code for FSM and rest of the entity ...

fsm_state(0 to 2) <= ... Signal 801 ...

```

8 5 3 { --!! Embedded FSM : examplefsm;
8 5 9 { --!! clock      : (fsm_clock);
8 5 4 { --!! state_vector : (fsm_state(0 to 2));
8 5 5 { --!! states      : (S0, S1, S2, S3, S4);
8 5 6 { --!! state_encoding : ('000', '001', '010', '011', '100');
      { --!! arcs        : (S0 => S0, S0 => S1, S0 => S2,
8 5 7 { --!!              (S1 => S2, S1 => S3, S2 => S2,
      { --!!              (S2 => S3, S3 => S4, S4 => S0);
8 5 8 { --!! End FSM;

```

END;

Fig. 8C

entity FSM : FSM

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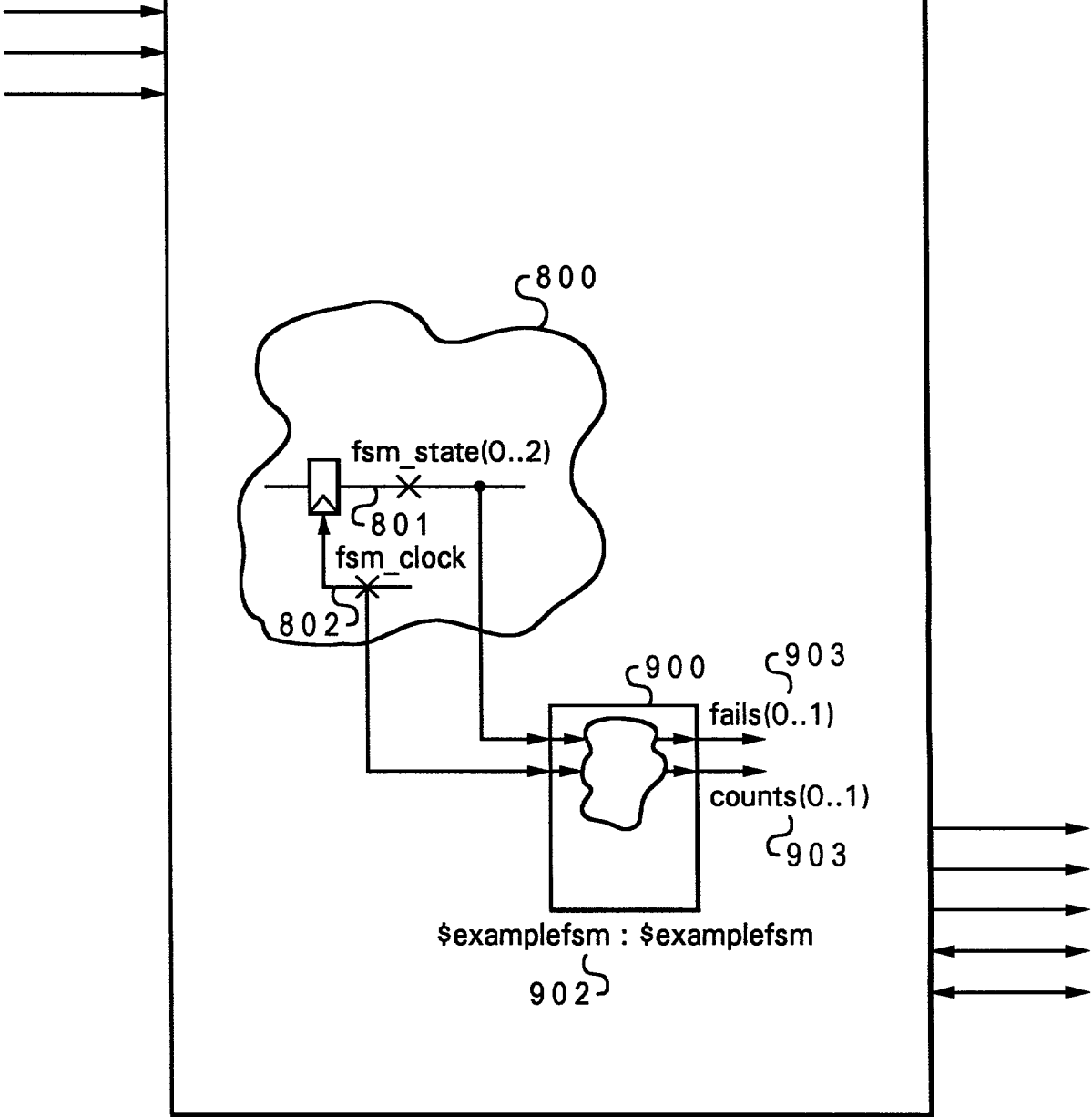
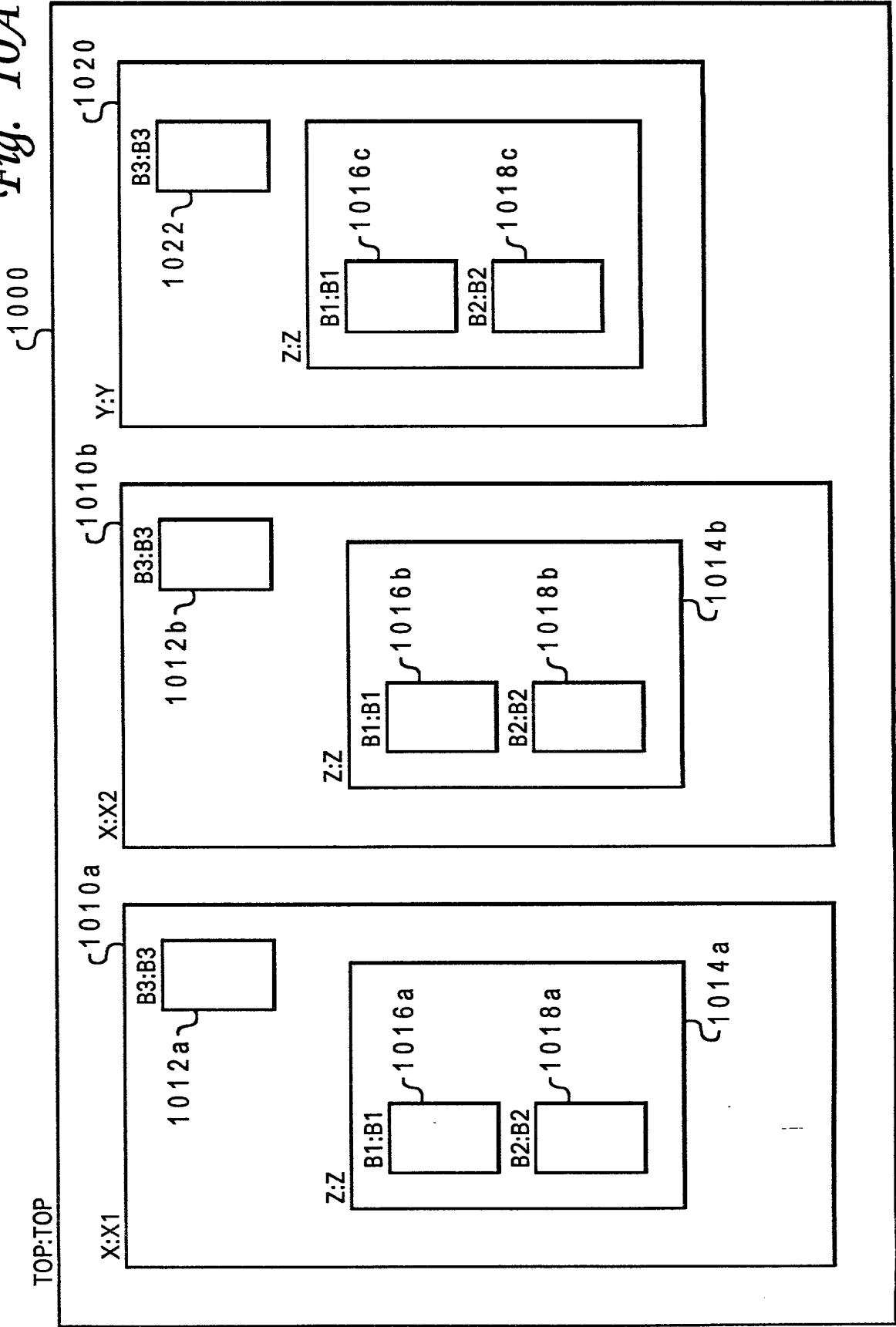


Fig. 9

Fig. 10A



$\underbrace{\text{<instantiation identifier> . <instrumentation entity name> . <design entity name> . <eventname>}}_{1030} \quad \underbrace{\phantom{\text{<instantiation identifier> . <instrumentation entity name> . <design entity name> . <eventname>}}}_{1032} \quad \underbrace{\phantom{\text{<instantiation identifier> . <instrumentation entity name> . <design entity name> . <eventname>}}}_{1034} \quad \underbrace{\phantom{\text{<instantiation identifier> . <instrumentation entity name> . <design entity name> . <eventname>}}}_{1036}$

Fig. 10B

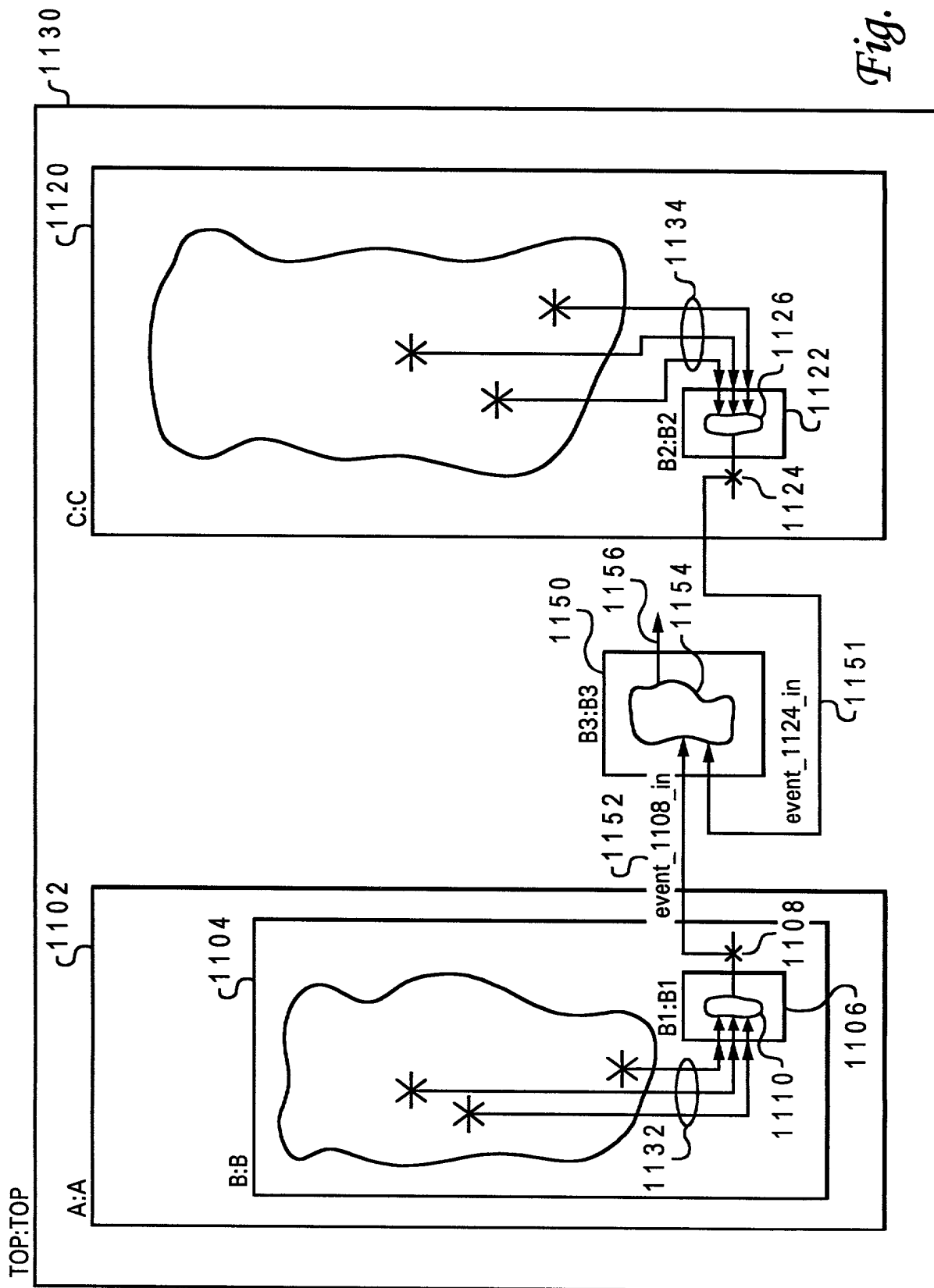
$\underbrace{\text{X1}}_{1030}$	$\underbrace{\text{B3}}_{1032}$	$\underbrace{\text{X}}_{1034}$	$\underbrace{\text{COUNT1}}_{1036}$	$\underbrace{\phantom{\text{COUNT1}}}_{1040}$
X1.Z	B1	Z	COUNT1	$\underbrace{\phantom{\text{COUNT1}}}_{1041}$
X1.Z	B2	Z	COUNT1	$\underbrace{\phantom{\text{COUNT1}}}_{1042}$
X2	B3	X	COUNT1	$\underbrace{\phantom{\text{COUNT1}}}_{1043}$
X2.Z	B1	Z	COUNT1	$\underbrace{\phantom{\text{COUNT1}}}_{1044}$
X2.Z	B2	Z	COUNT1	$\underbrace{\phantom{\text{COUNT1}}}_{1045}$
Y	B4	Y	COUNT1	$\underbrace{\phantom{\text{COUNT1}}}_{1046}$
Y.Z	B1	Z	COUNT1	$\underbrace{\phantom{\text{COUNT1}}}_{1047}$
Y.Z	B2	Z	COUNT1	$\underbrace{\phantom{\text{COUNT1}}}_{1048}$

Fig. 10C

$\underbrace{\text{<instantiation identifier> . <design entity name> . <eventname>}}_{1030} \quad \underbrace{\phantom{\text{<instantiation identifier> . <design entity name> . <eventname>}}}_{1034} \quad \underbrace{\phantom{\text{<instantiation identifier> . <design entity name> . <eventname>}}}_{1036}$

Fig. 10D

Fig. 11A



--!! Inputs
 --!! event_1108_in <= C.[B2.count.event_1108];
 --!! event_1124_in <= A.B.[B1.count.event_1124];
 --!! End Inputs

1163 } 1165 }
 1164 } 1166 }
 1161 }
 1162 }

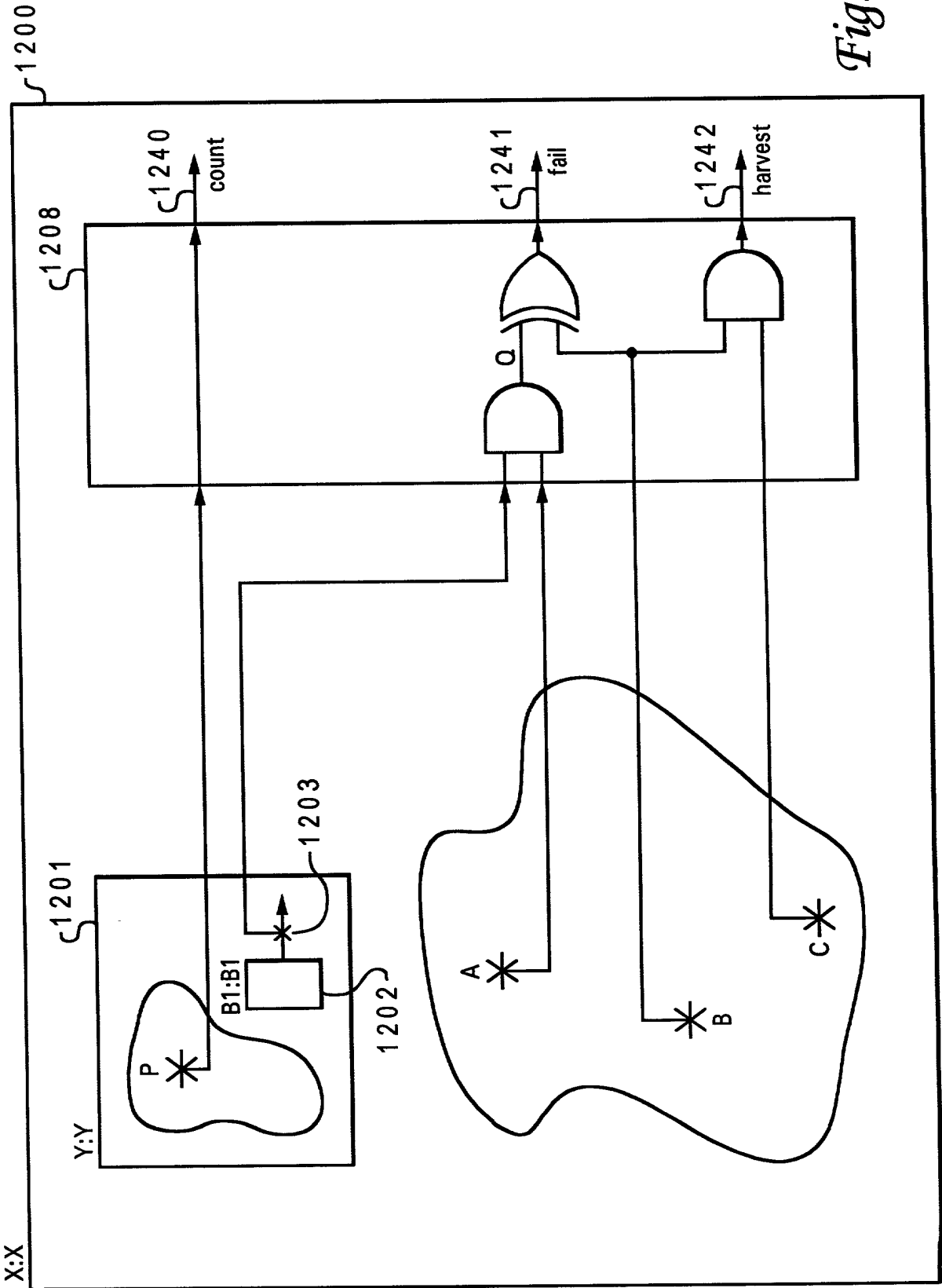
Fig. 11B

--!! Inputs
 --!! event_1108_in <= C.[count.event_1108];
 --!! event_1124_in <= B.[count.event_1124];
 --!! End Inputs

1171 }
 1172 }

Fig. 11C

Fig. 12A



```

ENTITY X IS
    PORT(
        :
        :
        :
    );

    ARCHITECTURE example of X IS
    BEGIN
        .
        .
        .
        .
        ... HDL code for X ...
        .
        .
        .
    END;

```

1 2 2 1 { Y:Y
PORT MAP(:
);

1 2 2 2 { A <=
B <=
C <=

1 2 2 3 { --!! [count, countname0, clock] <= Y.P; 1 2 3 0
--!! Q <= Y. [B1.count.count1] AND A; 1 2 3 2
--!! [fail, failname0, "fail msg"] <= Q XOR B; 1 2 3 4
--!! [harvest, harvestname0, "harvest msg"] <= B AND C;
END; 1 2 3 6

1 2 2 0

Fig. 12B